AI-Driven Co-Optimization of Design and Manufacturing for Heterogeneous AI Chips

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The efficiency of data movement between dies, whether mounted or stacked on silicon or glass substrates, is heavily influenced by the electro-thermo-mechanical properties of the interconnects and the bonding techniques used. Conventional evaluations of these materials and technologies often rely on metrics such as resistivity, coefficient of thermal expansion, Young's modulus, pitch, and interconnect width. However, these parameters do not directly correlate with critical system-level metrics such as performance, power consumption, and area efficiency.

In this presentation, we introduce AI/ML-based approaches to accurately and efficiently model the relationship between manufacturing properties and system performance. We demonstrate how these models enable co-optimization of manufacturing and system design, with a focus on heterogeneous chip architectures for AI accelerators. By leveraging predictive analytics, we aim to bridge the gap between materials science, advanced packaging, and system architecture—driving the next wave of semiconductor innovation for AI applications.